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IC-CAD tools to show dazzling advances

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6/14/1999 02:35 PM EDT

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EDA industry leaders and high-profile startups are not the only exhibitors showing off deep-submicron IC breakthroughs at next week's Design Automation Conference. An array of new and existing companies will field solutions in such areas as automated transistor-level layout, cell-library power optimization and characterization, and RAM design and optimization.

A first-time DAC exhibitor is Cadexterity (Santa Clara, Calif.), which will demonstrate the first production version of its Design-Driven Layout System. This tool suite incorporates automatic layout generation, high-level device-based editing and process-migration technology. It is intended to compete with Cadence Design Systems Inc.'s Virtuoso product.

The layout can be automatically generated from a Spice net-list, or from a schematic design built with the company's schematic editor. Cadexterity claims the product can achieve handcrafted quality through operations such as device merging, folding, bending, splitting, diffusion cutting and automatic guard-ring insertion.

"We can increase productivity by an order of magnitude," said Craig Harris, chief technical officer at Cadexterity. A key advantage, he said, is the use of "smart devices," such as transistors, that can modify themselves and merge with other elements. The Design-Driven Layout System is available now on Windows NT platforms and is being ported to Unix at a list price of $150,000.

Another schematic-driven layout editor that promises a high level of automation is Max-LS, an offering from Micro Magic Inc. (Sunnyvale, Calif.). The product features interactive layout generation, real-time design-rule checking and schematic-to-layout cross-probing.

Richard Smith, senior technology adviser at Micro Magic, noted that the ability to see and compare schematic and layout information existed in earlier CAD systems but has been lost in recent releases from Cadence and Mentor Graphics Corp. Max-LS claims to restore that capability. The product will be available on Solaris and Linux platforms in the third quarter for $50,000.

Much attention will be paid at DAC to the creation, optimization and characterization of cell libraries. Startup Prolific Inc. (Newark, Calif.) will announce its ProGenesis tool suite for cell-library creation. Paul de Dood, president of Prolific, said the tool allows "complete control" over any arbitrary layout.

ProGenesis lets users create cell libraries through design synthesis, custom layout, GDSII migration or a library of pre-packaged generators. The design-synthesis capability creates cell generators from Spice net-lists by identifying logical structures for placement and routing. A visual editor lets users graphically create or edit cell generators. Detailed placement, routing and compaction are also available. Pricing starts at $175,000 on Unix or Linux platforms.

To address the problem of cell-level power management, Library Technologies Inc. (Saratoga, Calif.) is announcing Cell-Opt, a dynamic circuit-level power optimizer. If users don't constrain the outputs, said company president Mehmet Cirit, the tool can reduce internal power dissipation by up to 30 percent.

To use the product, designers provide a Spice net-list, functional circuit description and information about loads the circuit will drive. CellOpt produces a new net-list with modified device sizes. CellOpt is available now on Unix workstations, starting at $80,000.

Power characterization
Silicon Metrics Corp. (Austin, Texas) will announce CellRater PCX, bringing power-characterization capabilities to its existing Rater Series of characterization and modeling tools. Users generate power models for use with synthesis and power-analysis tools. Available now on Unix platforms, it starts at $58,000.

Circuit Semantics Inc. (San Jose, Calif.) will introduce DynaCell, which automatically characterizes cell libraries for various EDA tools. DynaCell generates simulation vectors for use with transistor-level simulators such as Avant!'s Star-HSpice and includes an HSpice-compatible simulation engine.

Tom Daspit, vice president of marketing, said the product extracts the function of the cell from Spice net-lists. From that extracted function, it automatically generates optimized simulation vectors. DynaCell is available now on Windows NT, Linux and Unix platforms. Pricing starts at $90,000.

OEA International Inc. (Santa Clara) has four new products at DAC: RAM Designer, Clock Designer, Ring Designer and P-Plan, a power-distribution networking tool. Of those, the most significant is RAM Designer, said Jerry Tallinger, vice president of marketing and sales. Working from Spice circuits, RAM Designer promises fast design, analysis and optimization of SRAM arrays. "This tool has the potential to save hundreds of hours of design time," Tallinger said. Starting at $30,000, it is available on Unix platforms.