DPC DataPath Compiler

- **Custom Performance with ASIC Effort**
- **3X Faster than ASIC**
- **40% Smaller than ASIC**
- **10X Less Effort than Full Custom**

The Tool for High Performance Designs

DPC is the tool used by designers needing high performance chips. They want the performance of full custom design, but with a much shorter design cycle. Datapaths designed with DPC are 3X (three times) faster and 40% smaller than synthesis and place and route. At the same time, it takes 10X (ten times) less effort than full custom design.

In deep sub-micron design, wire length is the dominant factor affecting critical path timing. Cell placement becomes a critical step in chip performance as well as power consumption. With traditional tools, designers are at the mercy of automatic placement tools. The DataPath Compiler (DPC) lets the designer control placement with immediate timing feedback. Multiple what-if experiments can be performed. Using a graphical display that back annotates timing to the schematic, you can easily identify timing problems and rapidly iterate through potential solutions, yielding faster results. DPC is so fast it can place, and then time, a 50K gate datapath in 2-3 minutes.

Useful Identification of Critical Paths

DPC predicts wire lengths early in the design cycle. The resulting timing iterations are both fast and accurate, allowing the designer to quickly iterate to their performance goal. The critical paths are displayed directly on the schematic at all levels of the design hierarchy. In addition, the actual delays of the paths are annotated onto the wires in both the schematic and placement view.

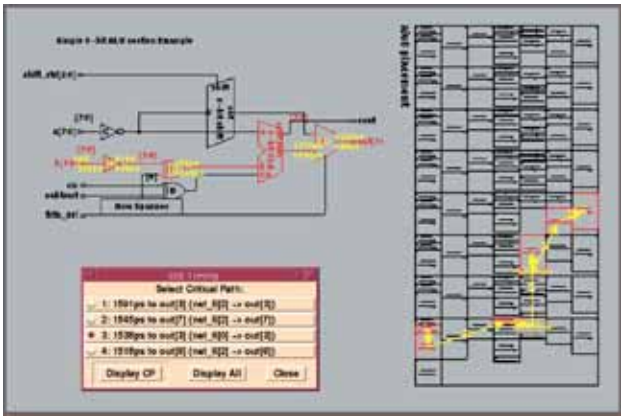

Figure 1-a.
The example above shows the placement generated for our sample 8-bit ALU. A critical path is highlighted in red and yellow on both the schematic an placement views. Timing for other nets is indicated in the menu and new nets can be selected and highlighted.

DPC for Critical Path Optimization

In datapath designs, some simple directives by the designer can produce speed-optimized layouts. These directives are easily given and modified in DPC. The placement of components on the schematic directs relative placement in the placement file.

Cells can also be hard placed at specific row or column locations and empty space can be indicated. DPC automatically generates the row and column placement and predicted wire lengths. Wire predictions can be used to drive the DPC timing analyzer as well as external timing analyzers inluding Pearl, PrimeTime and PathMill.

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DPC reads the output from static timing analysis and displays the critical paths directly on the schematic. The placement can be modified to optimize critical paths, or extra drivers can be added to the critical path, all in the schematic. You then run through the placement and timing iteration again. This iteration continues until the timing criteria are satisfied. The iteration loop is fast and visual. When you are satisfied with the design performance, the placement file (DEF file) is passed to a routing tool. The routed result can then be read into the MAX Layout Editor to view, and edit if necessary.

DPC Design Flow

With DPC, you first enter the schematics into the SUE design manager. DPC then uses the schematic as a seed for placement. Once DPC has the placement, it is able to estimate the wiring delays and send this info to a static timing analyzer. The results of static timing analysis are then read back into SUE. The critical path is highlighted in both the schematic and placement view. Additionally, the delay and slope at each node are displayed.

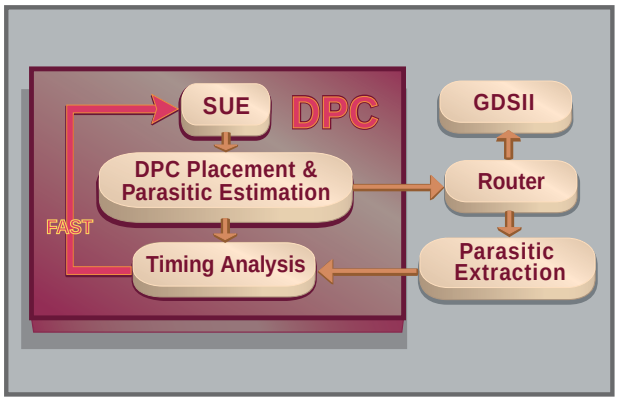

Figure 2-a.
DPC reduces the time required for placement and timing analysis from days to minutes.

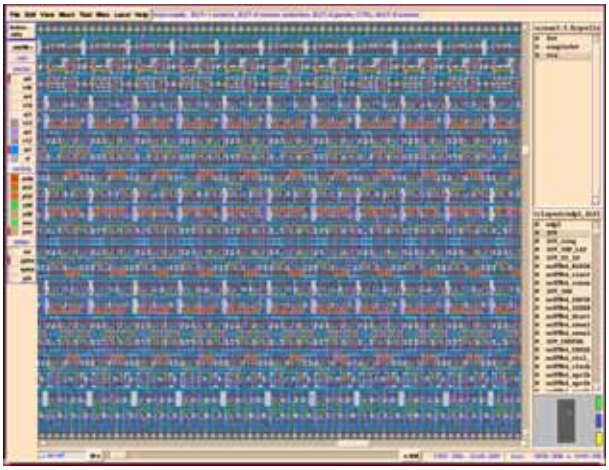

Figure 2-b.
The DEF placement file is sent to a router. The resulting GDSII file can then be read into MAX (Micro Magic's layout tool).

DPC Features:

- Automatically route, generate parasitics, run timing analysis, and display critical-path timing directly on schematics.
- DPC includes its own timing analyzer, or you can use iintegrated static timing analysis tools such as Pearl, PathMill and PrimeTime.
- Fast - can do a 50K gate data path in a few minutes.
- Use standard cells or custom datapath cells.
- Write out DEF placement information and Verilog netlist for integration with routing tools.
- Available on LINUX platforms.

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