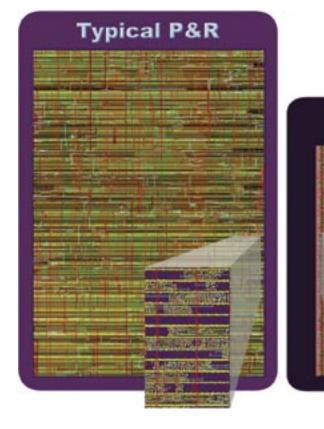
DFaster, Smaller, Lower Power

DPC

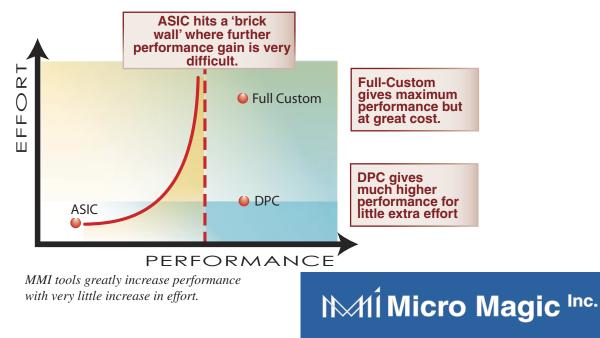
Use DPC to Make your Datapaths Faster,



Using DPC, engineers have produced real designs that were 3X faster, 40% smaller, and 40% lower power than their existing place & route design.

Smaller, Lower Power, Easy to Route

- Place, route and time 100K gates per minute.
- Regular bit-slice placement reduces congestion and wire length, reducing size and power.
- Gate Auto-sizer automatically improves timing and power.
- Uses all existing standard cell libraries.
- OpenAccess compliant.



Custom Performance with ASIC Effort

Greater Designer Control

HIGH-PERFORMANCE DATAPATHS

DAYS

Control Your Placement

DPC gives the designer

datapath. You control relative

placement for specific gates.

complete control of the

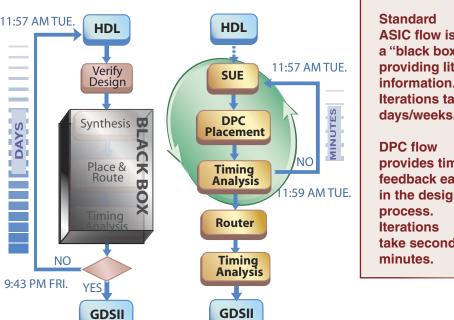
placement of gates, and

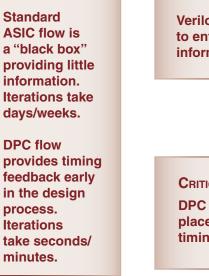
you can designate exact

HOW DPC SOLVES THE **POWER/PERFORMANCE PROBLEM:**

- 1. Import design data using schematics or Verilog.
- 2. Creates custom-like bit-slice placement which reduces congestion and improves routing.
- 3. Performs postplacement timing analysis.
- 4. Computes critical paths and provides timing information at each node.
- 5. Auto-sizes gates based on your constraints (optimizing for timing and power, or power alone).
- Modify your design 6. and see the new results very quickly. Iterations are done in minutes – DPC **computes 100.000** gates per minute.
- Checks for "hot spots" 7 with congestion analysis.
- 8. Outputs a DEF placement file for your existing P&R flow.
- Verifies timing post-9. route, and shows results graphically.







Verilog or Schematics to enter design information. section in the share's sector in the sector is the sector PRE 1 C. D.A. B. 41 CRITICAL PATH ANALYSIS **Wellect Ontical Part** ($10^{10} \text{ ps to out}[3]$ (ref_ $0[2] \rightarrow out[3]$) **DPC** computes as to out[7] (net_6[2] -> out[7]) placement, route, and o out[3] (net 時間 -> out[3]) to out[6] (net_6[2] -> out[6]) timing information. Display CP Display All Close

Control Your Gate Sizing

DPC automatically sizes the gates in your datapath, using a production-proven algorithm to select optimal sizes for speed, power or both. Using the "power down" option, Auto-Sizer will only down-size gates in order to minimize power required. At your option, you can also manually resize gates.

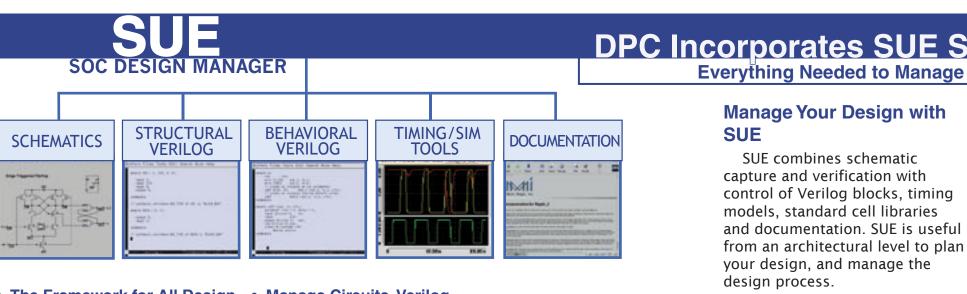
Timing Information and Critical-Path Analysis

DPC provides immediate timing feedback for placement and gate sizing. Multiple what-if experiments can be performed in seconds. Using a graphical display that back annotates timing to the schematic and placement file, you can easily identify timing problems and

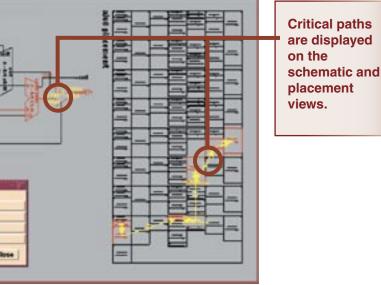
rapidly iterate through solutions. DPC is so fast it can place, route, and time a 100,000 gate datapath in one minute.

Design Inputs

DPC reads your Verilog and produces a schematic. For designers who don't use schematics, there is a "Verilog-



- The Framework for All Design Capture, Simulation, Timing and Data Management
- Manage Circuits, Verilog, **Documentation and Version Control**
- Fast and Effective Schematic Capture Tool
- Supports Industry **Standard File Formats**



Only" option. Once you are meeting your timing and power goals, you can use the built-in congestion analyzer to check for hot spots. Due to the regular bitslice placement and congestion check, DPC blocks usually route correctly on the first pass.

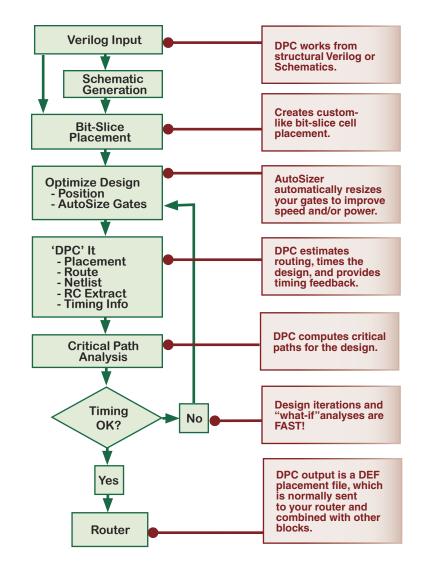
A DEF placement file and the Verilog netlist is sent to your router.

DPC Incorporates SUE SoC Design Manager Everything Needed to Manage Today's SoC Design Flow

- » Provides an architectural overview of your design.
- » Fully hierarchical, SUE can drill down to gate-level or transistorlevel detail of any block.
- » Structural Verilog is imported and automatically arranged as a schematic.
- » Enter your designs guickly with the simple graphical user interface.
- Drives Most Verilog and SPICE Simulators

DPC Features

- Up to 300% Faster Datapath Performance, 40% Lower Power, 40% Less Area.
- Custom performance with ASIC effort.
- Quickly builds custom-like datapaths using all existing standard cell libraries.
- DPC includes its own timing analyzer, or you can use PrimeTime[®].
- Fast processes 100,000 gates per minute.
- Writes DEF placement information and a Verilog netlist for integration with routers.
- Available on LINUX.



SUE Features:

- » Draw, view, and edit schematics, icons, graphics, and text.
- » Automatically:
 - » Attach Verilog models and documentation to schematics.
 - » Generate Verilog from schematic symbols and vice versa.
 - » Generate layout when used with MAX-LS Layout System.
- » Highlight nets and cross-probe between layout and schematic.
- » Maintain multiple views (behavioral, RTL, structural) of schematics.
- » Interactive cross-probing during simulation on schematic or waveform tool.
- Micro Magic, Inc. Sunnyvale, CA USA Phone: 408. 414. 7647 www.micromagic.com

- » Includes waveform viewer.
- » Reads/writes OVI compliant Verilog files.
- » No Vendor Lock-in from proprietary file formats or encryption. ASCII database for transportability and ease of use with other programs and revision control.
- » OpenAccess compliant.
- » Standard netlist and simulator interfaces.
- » Complete Tcl/Tk programming interface and API.

Micro Magic Inc.

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