3-Dimensional Integrated Circuit for Cellular Automata

December 4, 2009

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Overview

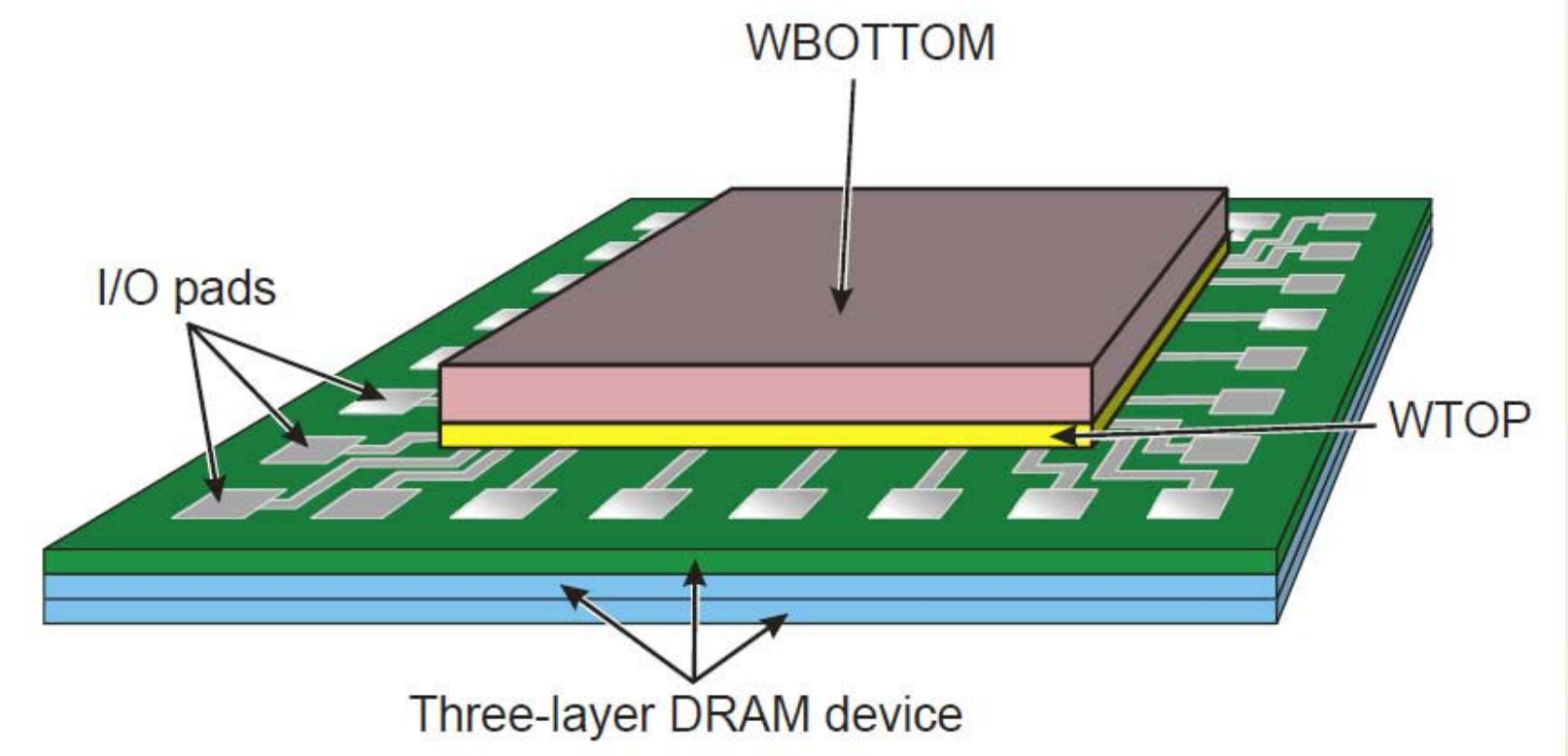
- Research Description
  - 3-D Integrated Circuit Technology (Tezzara®)
  - Cellular Automata (CA)
- Design
- Schedule
- Status
  - Tools
  - Layout
  - External Information
- Testing

Research Description – 3-D Integrated Circuit Technology (Chartered)

- Chartered Semiconductor Manufacturing Ltd.
  - 130nm
  - 5mm x 5mm Die
  - 6 Metal
  - 1.5V Logic
  - 2.5V Input/Output

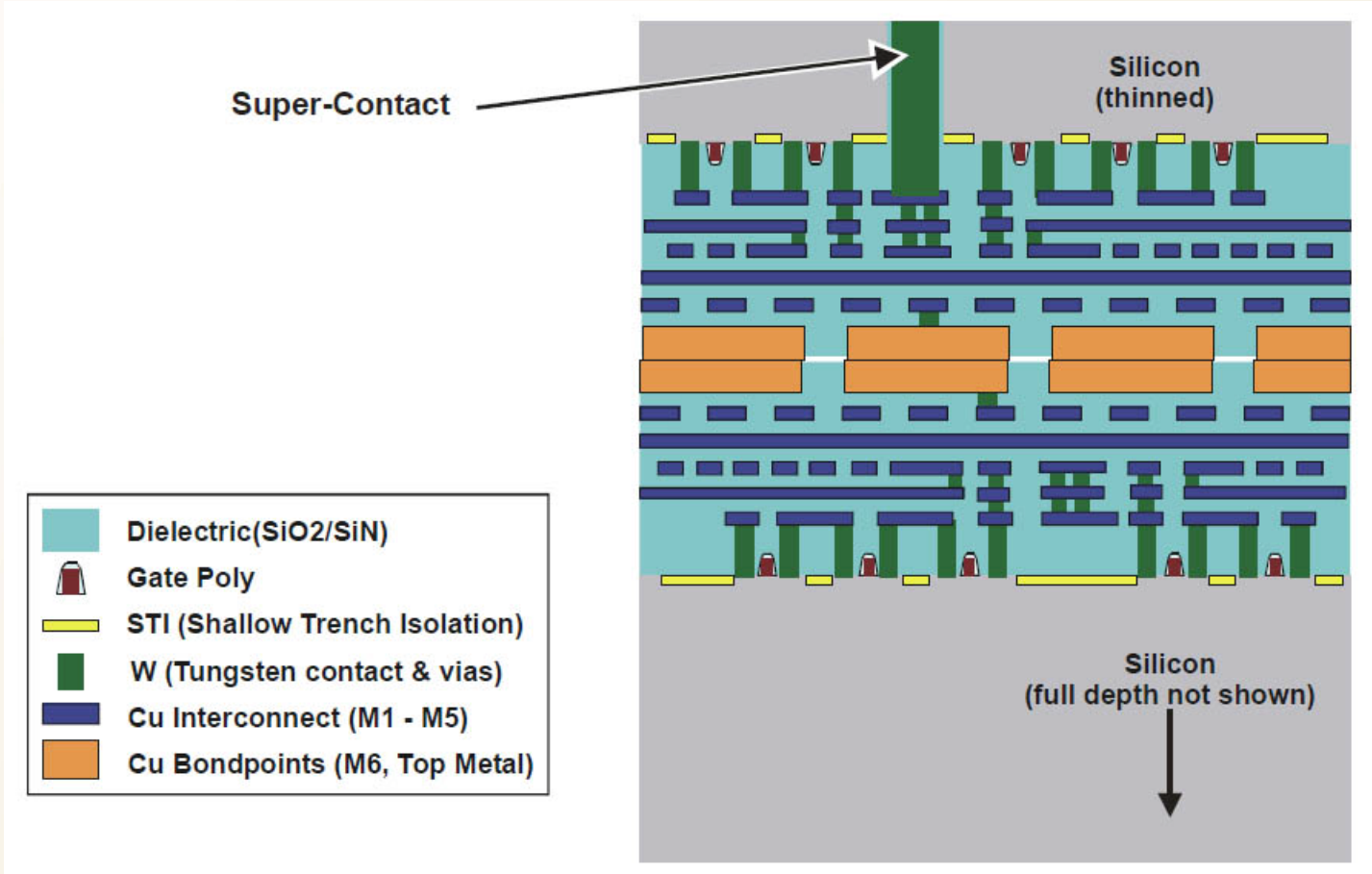
Research Description – 3-D Integrated Circuit Technology (Tezzaron®)

- Tezzaron® Semiconductor Final Configuration



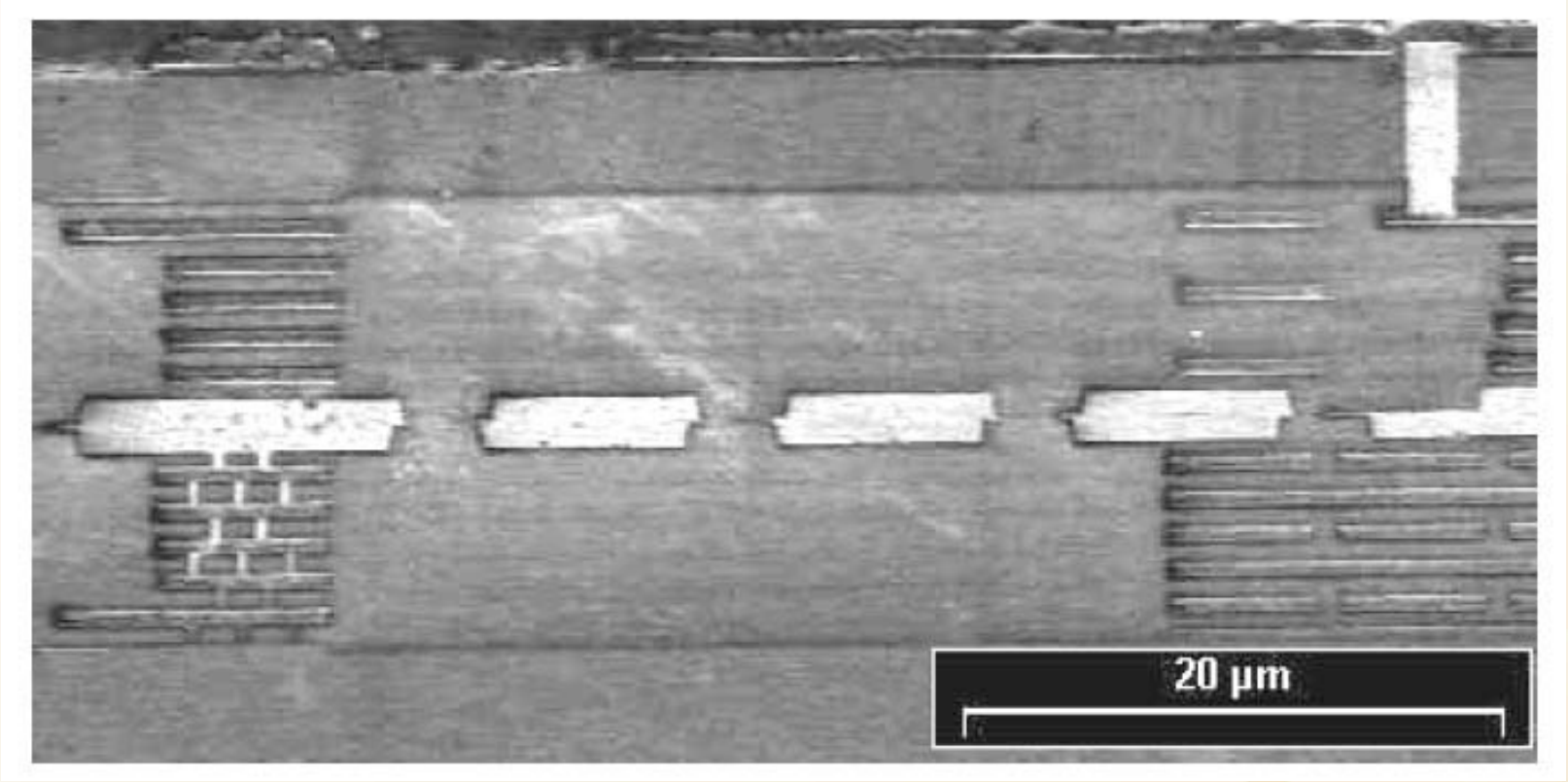
Research Description – 3-D Integrated Circuit Technology (Tezzaron®)

- Tezzaron® FaStack™ Process



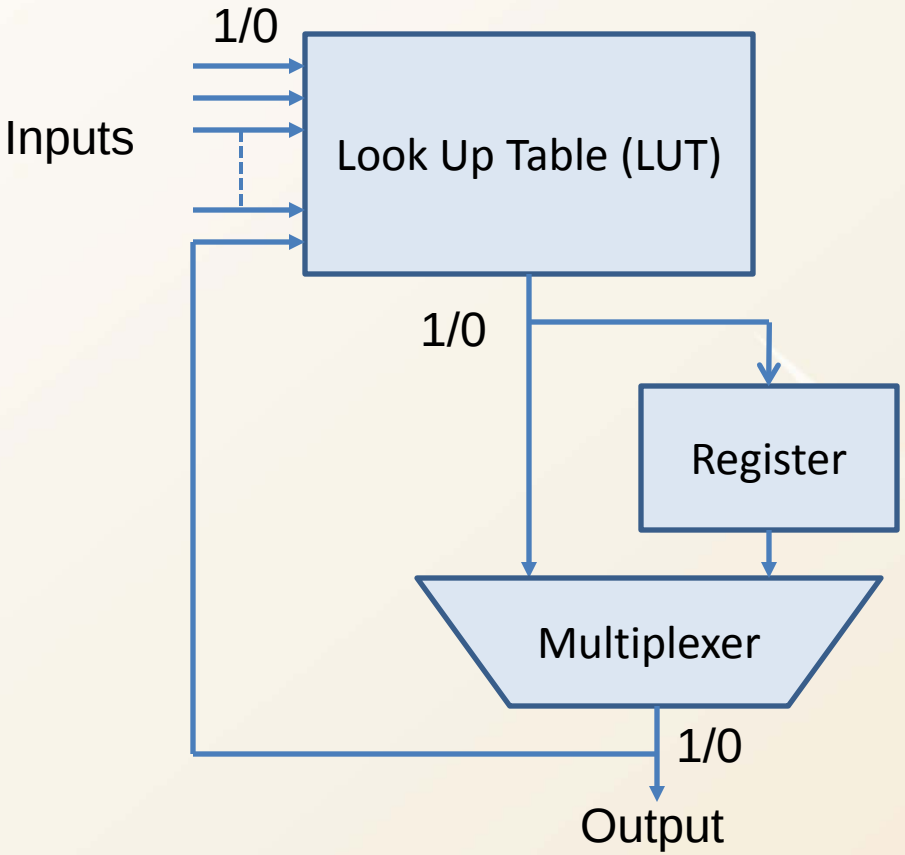
Research Description – 3-D Integrated Circuit Technology (Tezzaron®)

- Tezzaron® FaStack™ Process



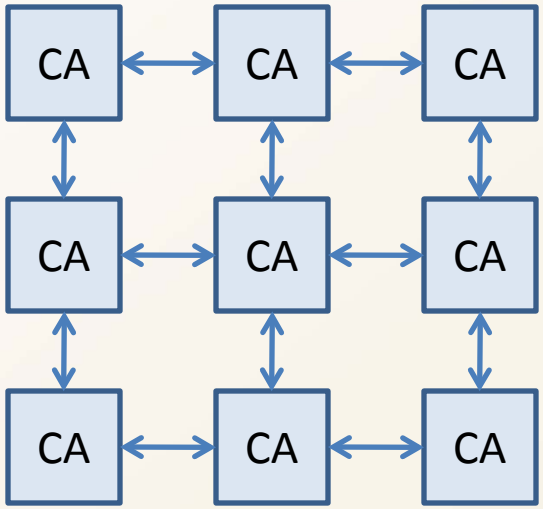
Research Description – Cellular Automata (CA)

- Two-State (Binary) Cellular Automaton

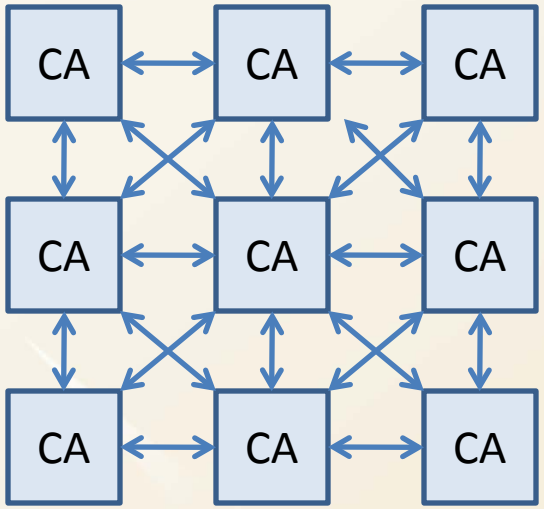


Planar CA Architectures

Linear
3 Neighbors
8 Patterns

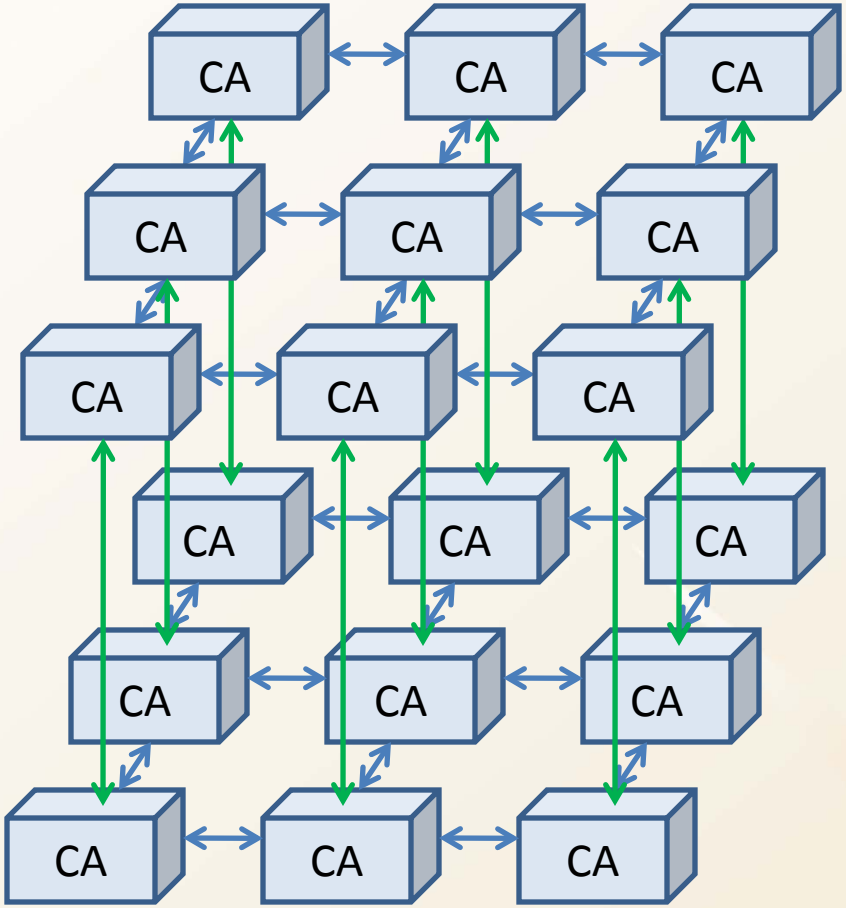


Orthogonal
5 Neighbors
32 Patterns



Adjacent
9 Neighbors
512 Patterns

3-Dimensional CA Architecture

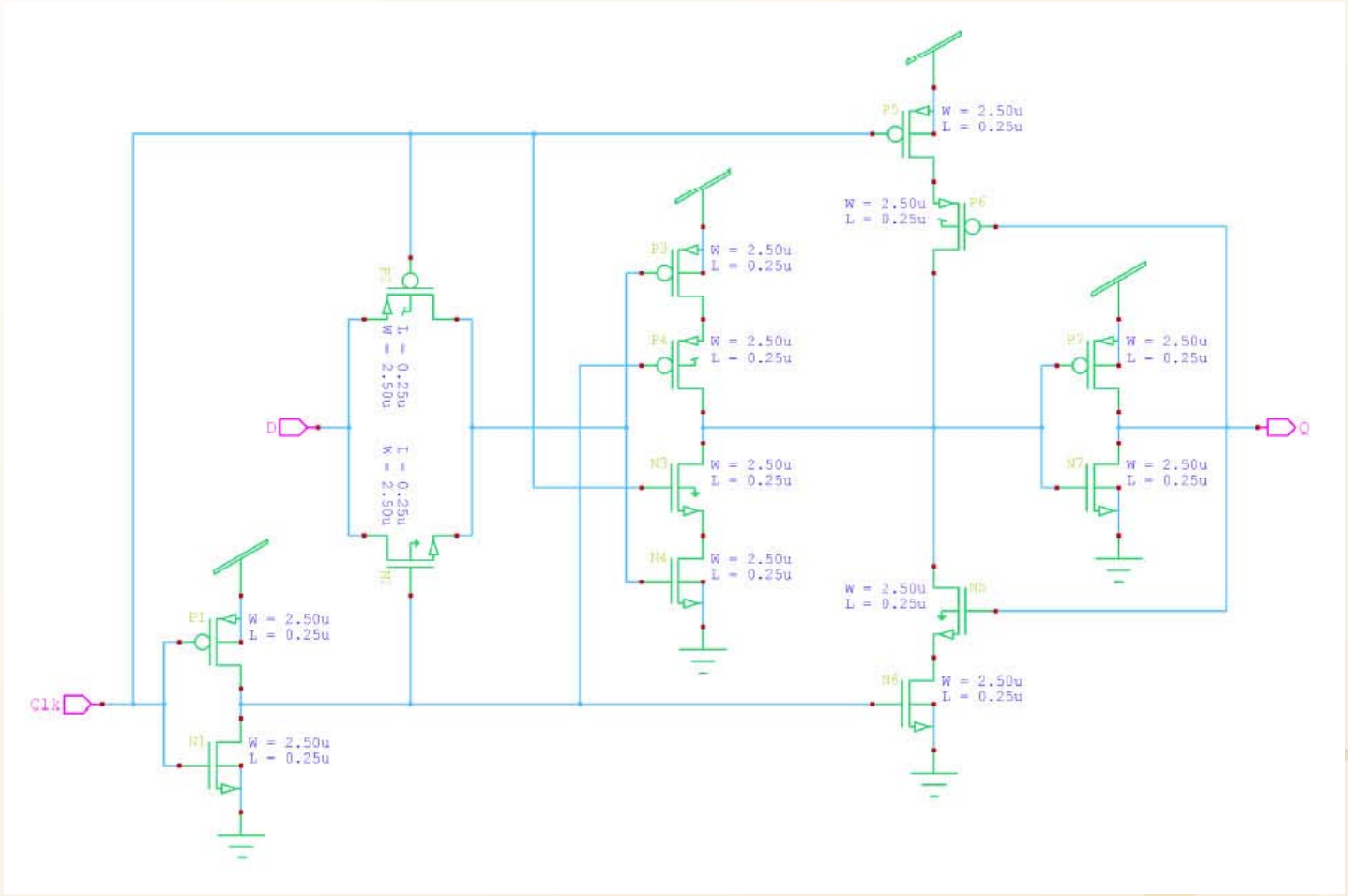


6 Neighbors
64 Patterns

CA Design

- Lookup Table
  - 64 D Flip-Flops with
    64:1 Multiplexer (6 Selector Inputs)
  - Serial Programming Connection of Flip-Flops
- Register
  - D Flip-Flop
- Final Multiplexer
  - D Flip-Flop for Programming in series with LUT
  - 2:1 Multiplexer

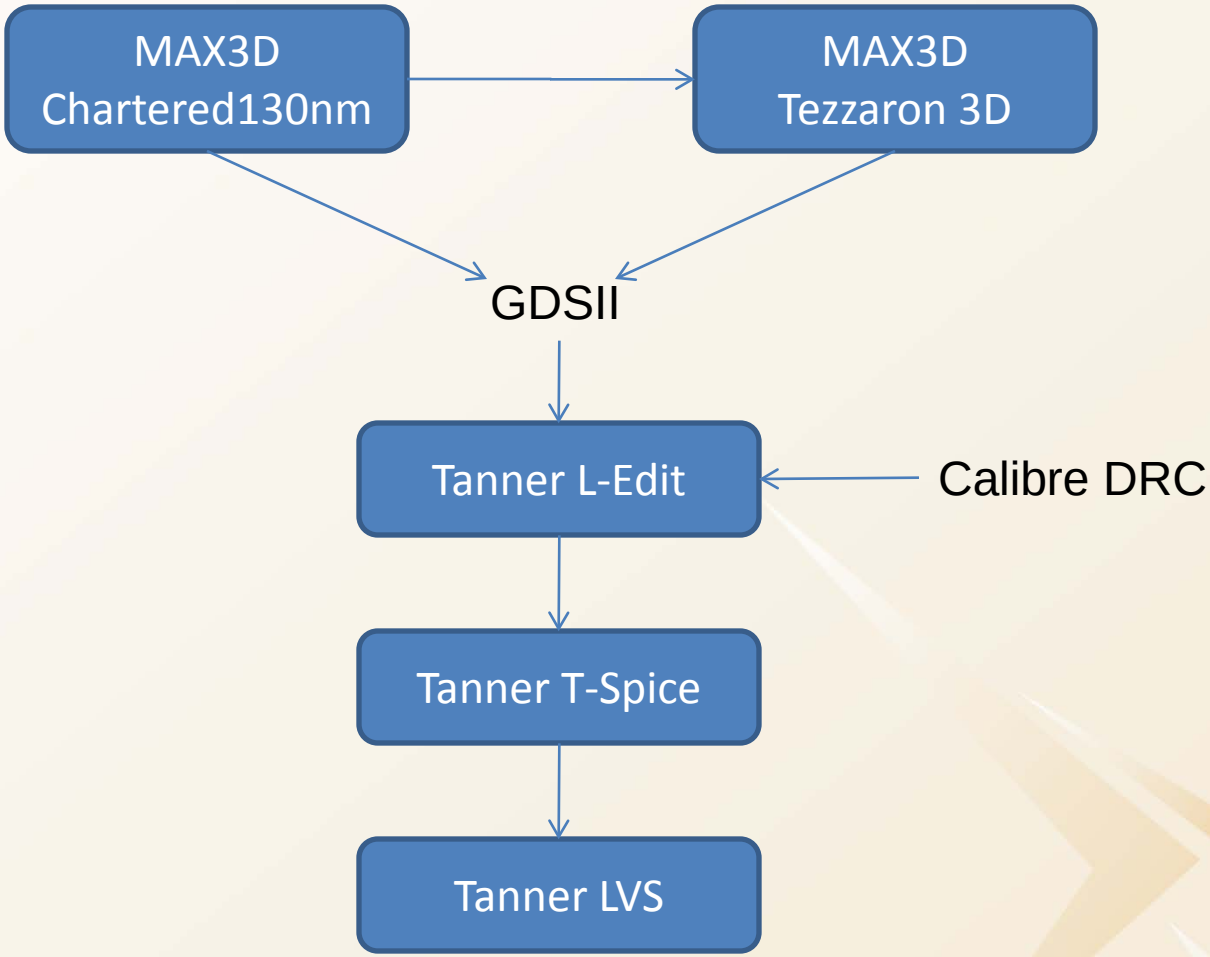
D Flip-Flop


P5
W = 2.50u
L = 0.25u
P6
W = 2.50u
L = 0.25u
P3
W = 2.50u
L = 0.25u
P4
W = 2.50u
L = 0.25u
P7
W = 2.50u
L = 0.25u
N3
W = 2.50u
L = 0.25u
N7
W = 2.50u
L = 0.25u
N4
W = 2.50u
L = 0.25u
N5
W = 2.50u
L = 0.25u
N6
W = 2.50u
L = 0.25u
P1
W = 2.50u
L = 0.25u
N1
W = 2.50u
L = 0.25u
T1
T2
D
Clk
Q

Schedule

• System Design	July – August 2009
• Schematic Design	August 2009
• Tool Integration	August – November 2009
• Layout	October 2009 – February 2010?
• Mock Tapeout	45 Days After Top Metal Specification
• Tapeout	60 Days After Top Metal Specification
• Fabrication	20 Weeks February – July 2010?
• Mounting	July – August 2010?
• Testing	August – November 2010?
• Report/Dissertation	December 2010

Tools

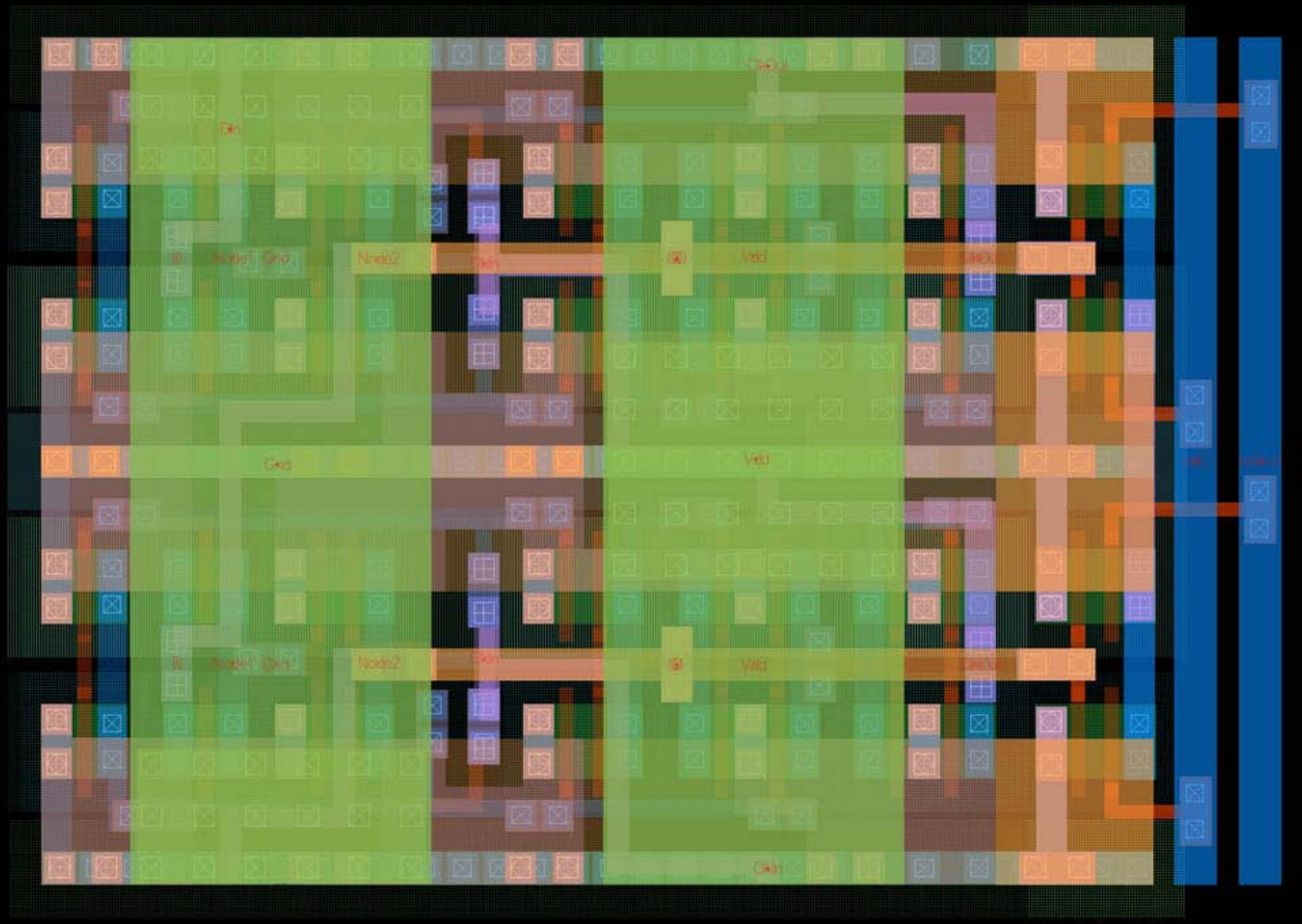

MAX3D
Chartered130nm
MAX3D
Tezzaron 3D
GDSII
Tanner L-Edit
Calibre DRC
Tanner T-Spice
Tanner LVS

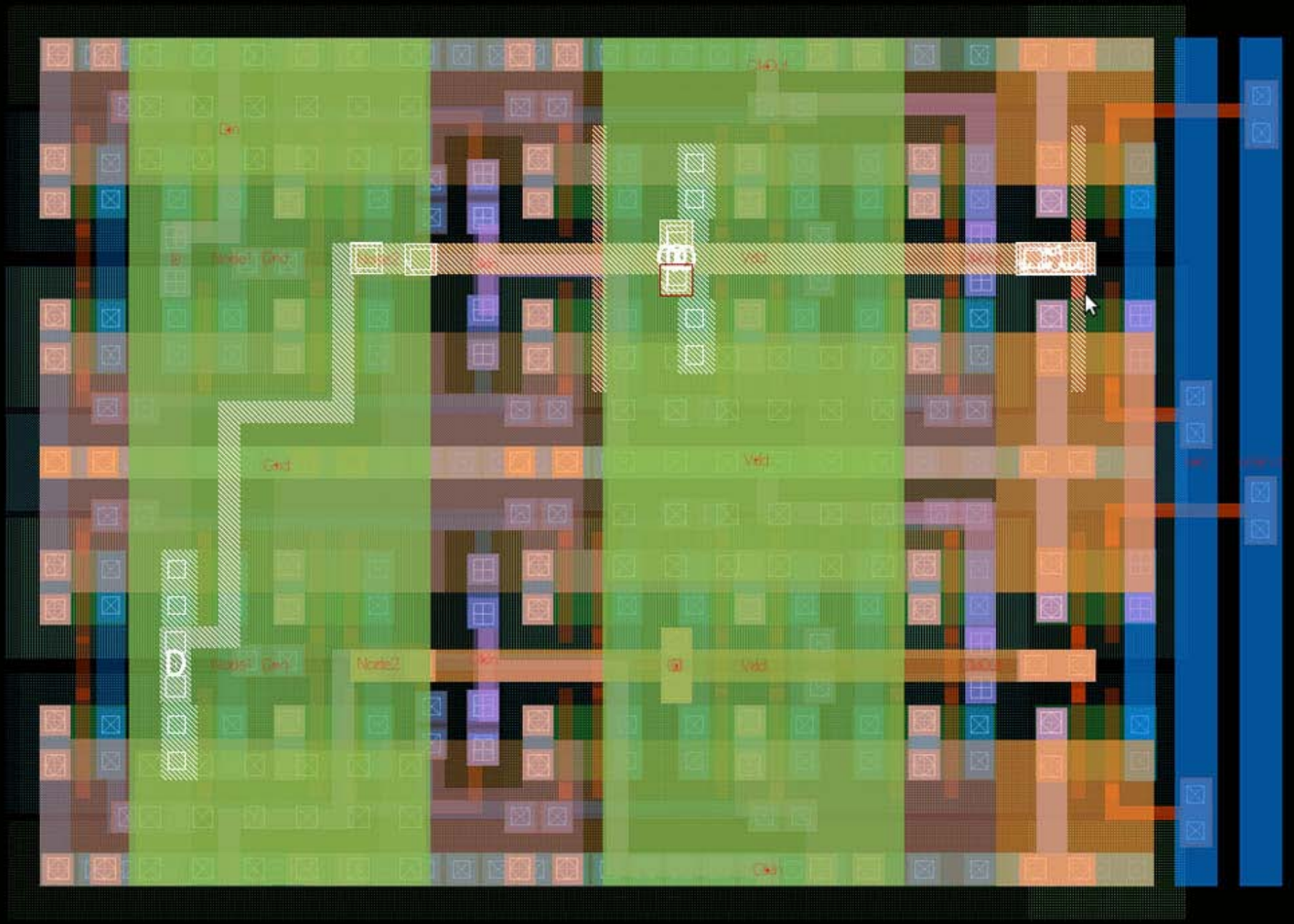
Tool Status

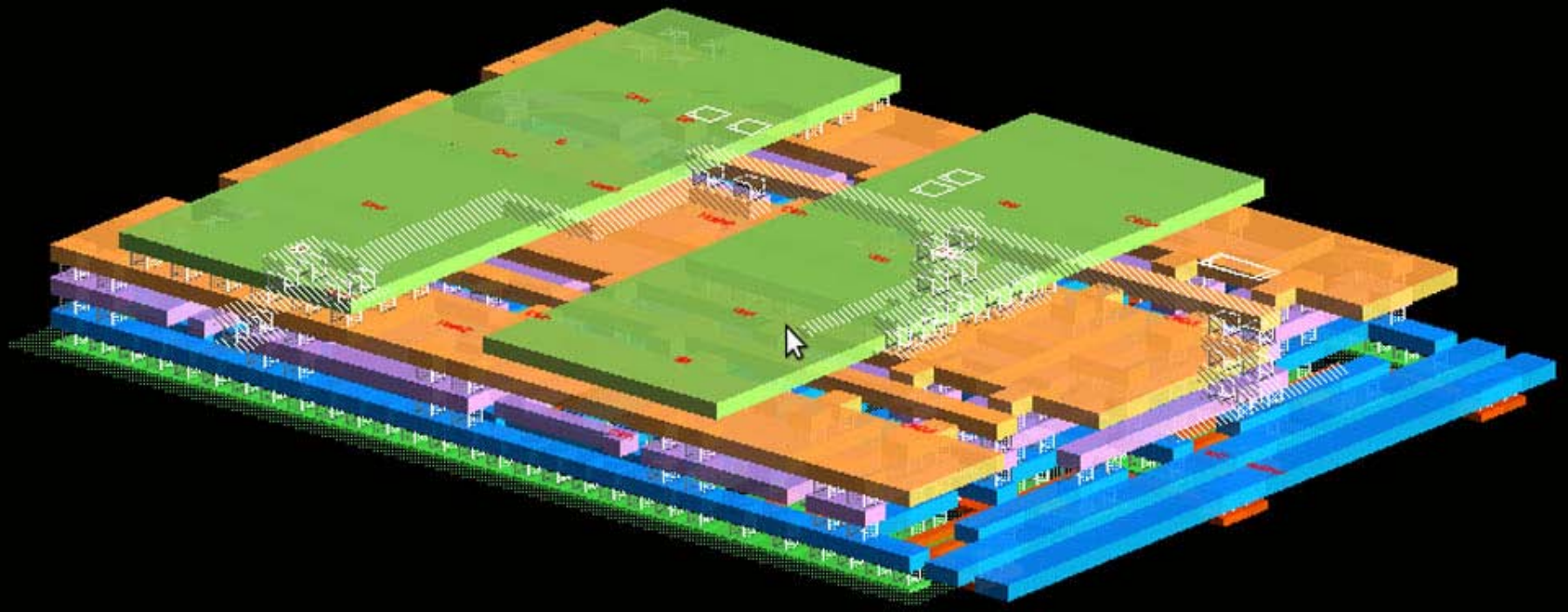
- Currently Using
  - Max3D with both technologies
  - Max3D GDSII output
  - L-Edit GDSII read
  - T-Spice simulation
  - Layout versus Schematic (LVS)
- Not Used Yet
  - Calibre® Design Rule Check (DRC)

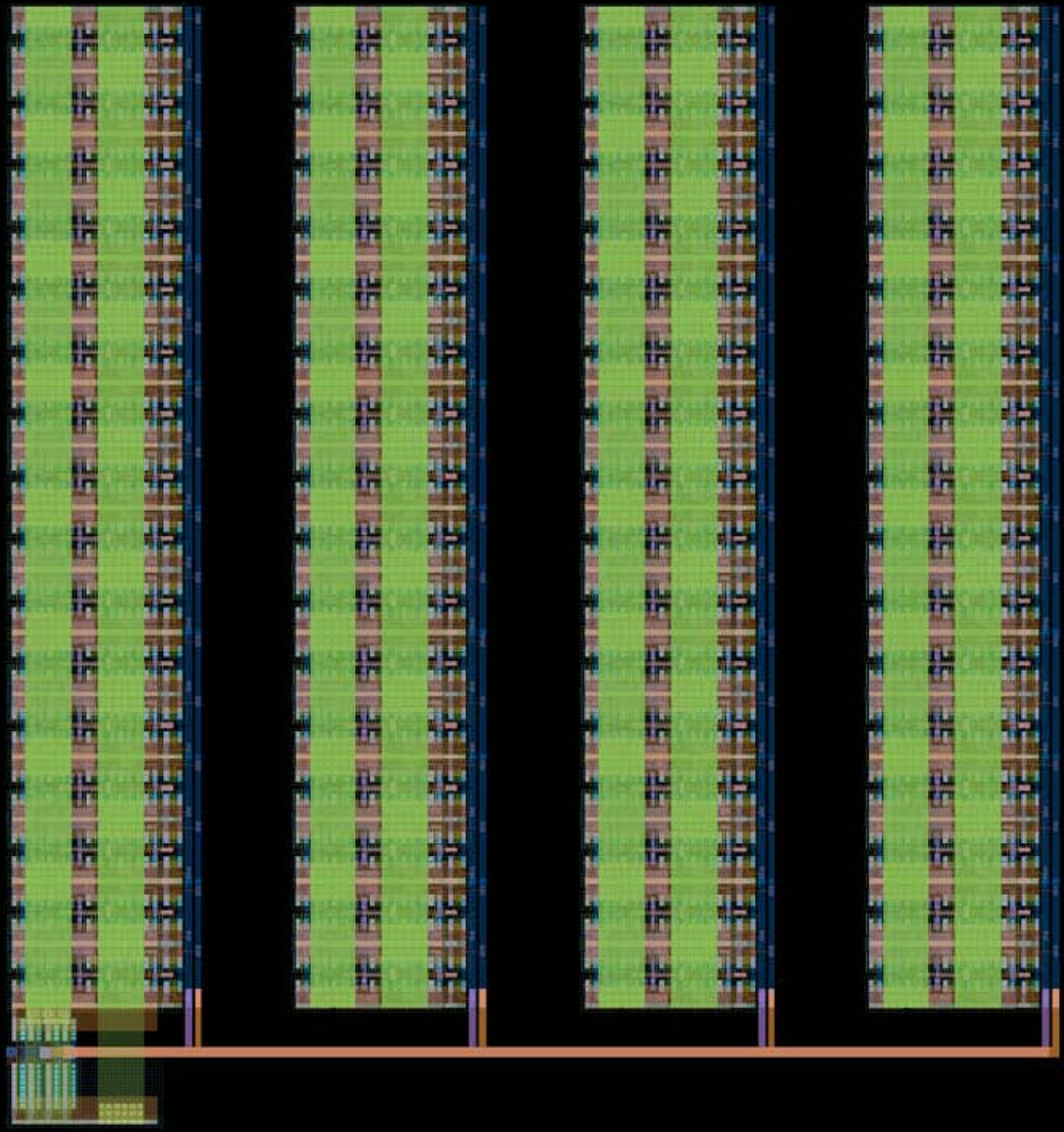
Layout

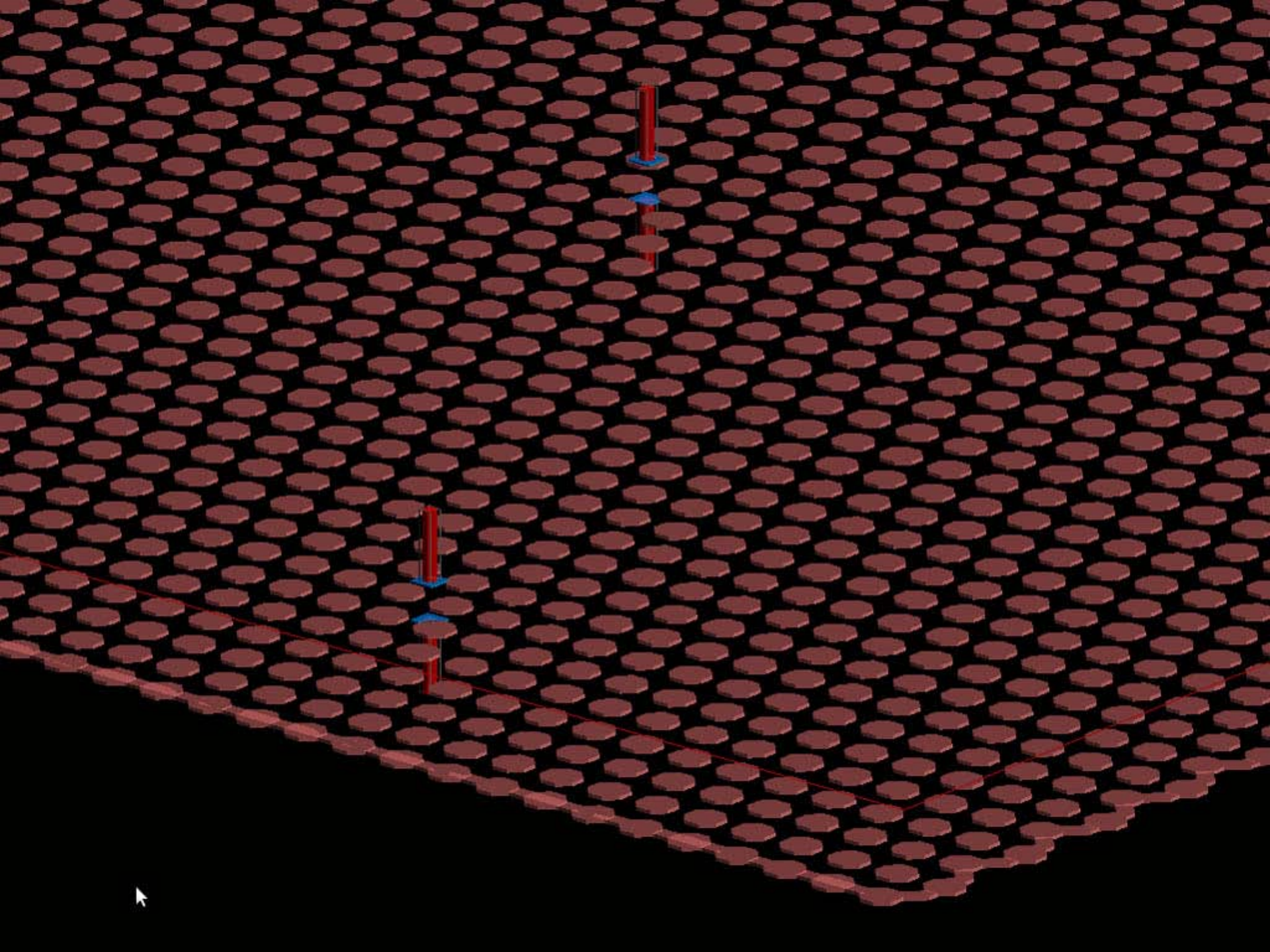
- Layout is performed with Micro Magic Max3D editor
- Final tapeout is two GDSII files
  - UNM_left
    - Connects to UNM_right through Metal 6
    - Connects to Memory and I/O using Through Silicon Vias (TSVs) to Back Metal that is bonded to Memory
  - UNM_right
    - Connects to UNM_left through Metal 6
    - Flipped right-to-left and placed on top of UNM_left

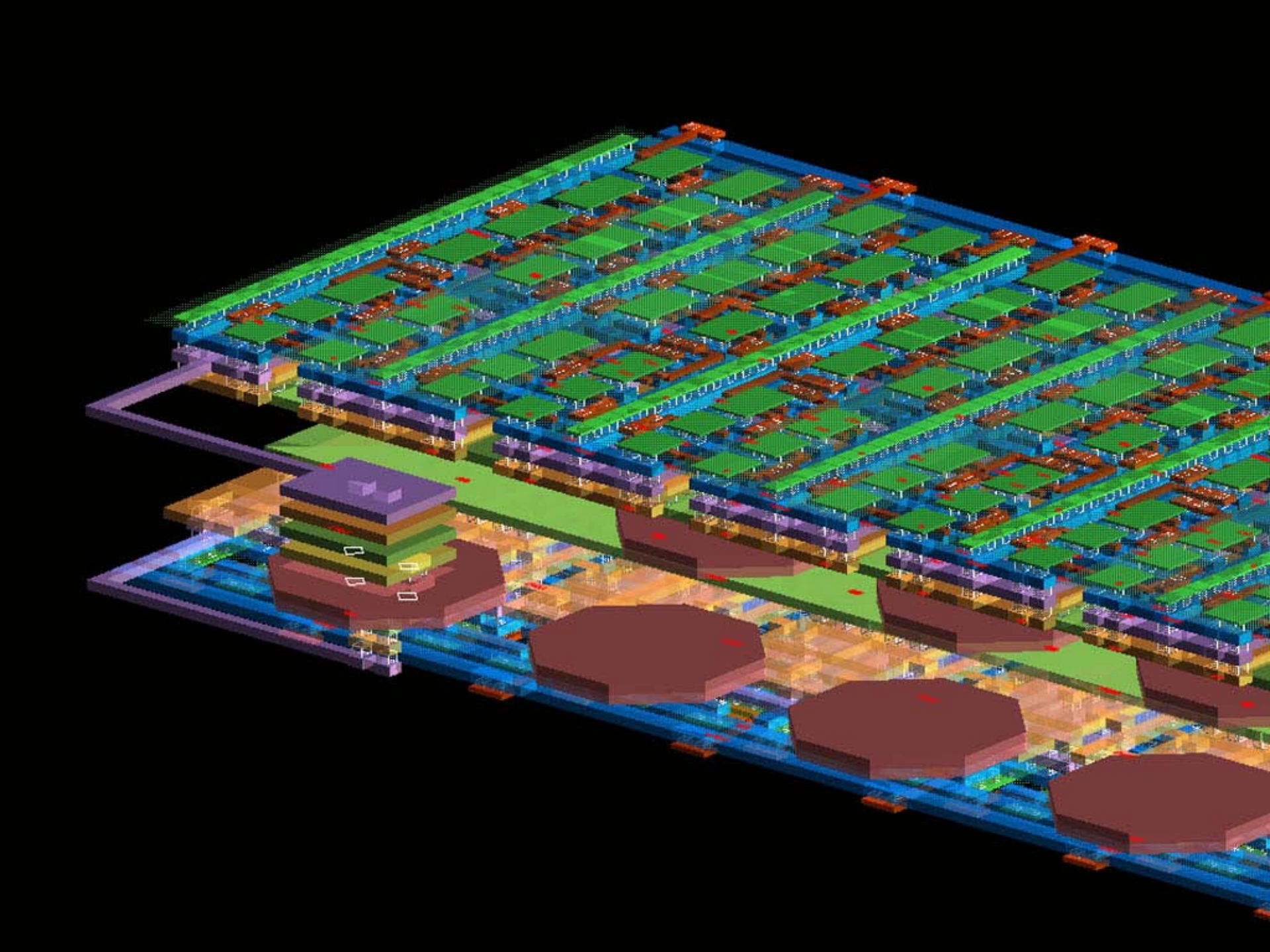

Vdd
Node2
Gnd
Vdd
Node2
Gnd
Vdd
Gnd

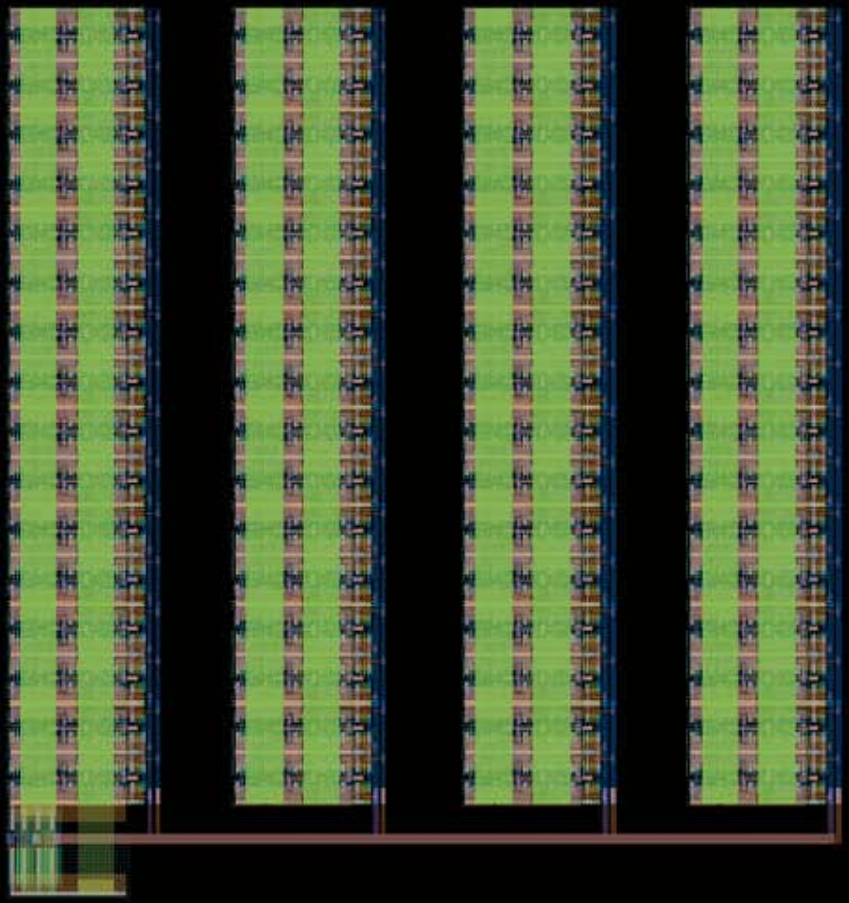

Gnd
Vdd
Node1
Node2

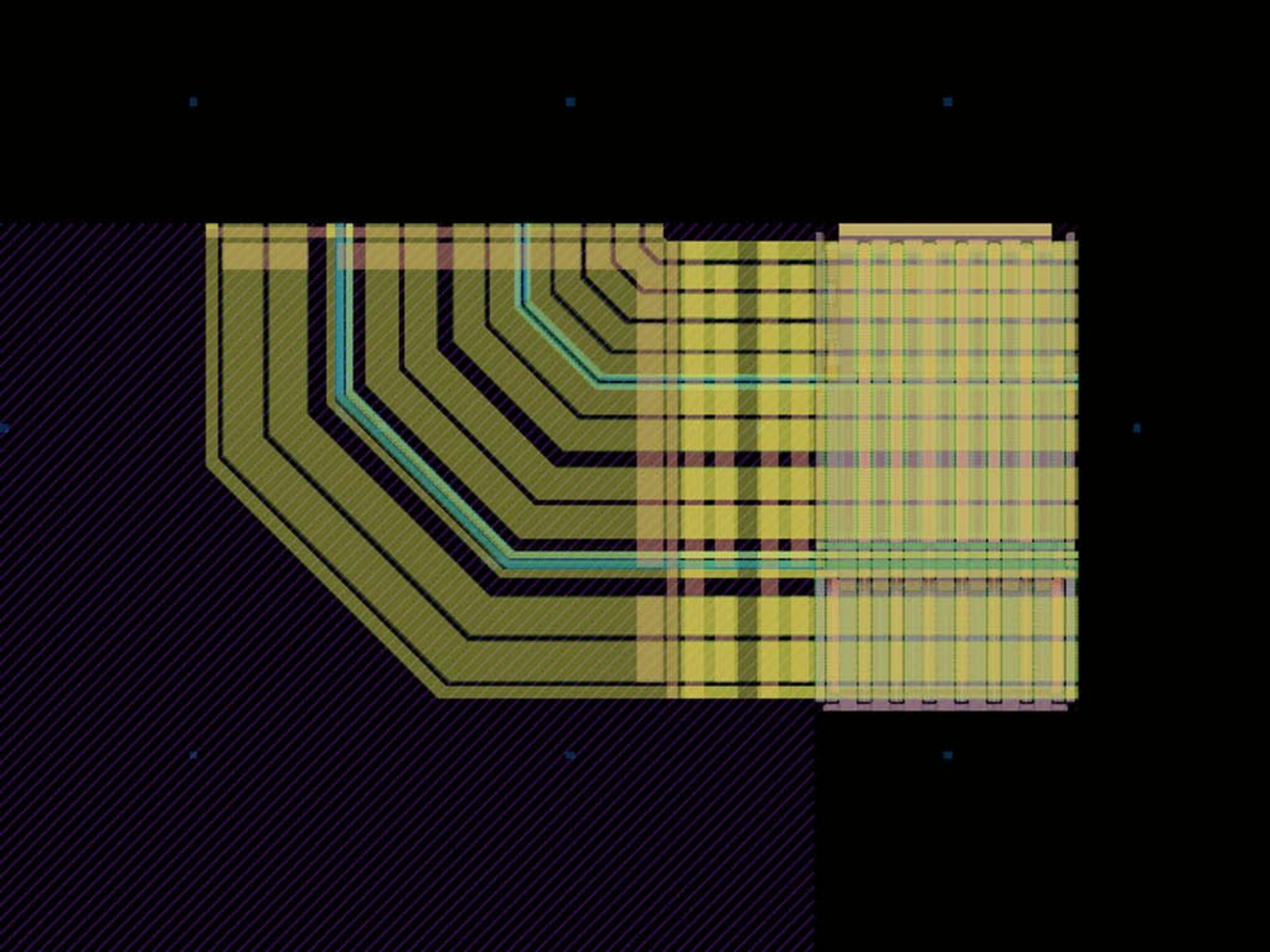


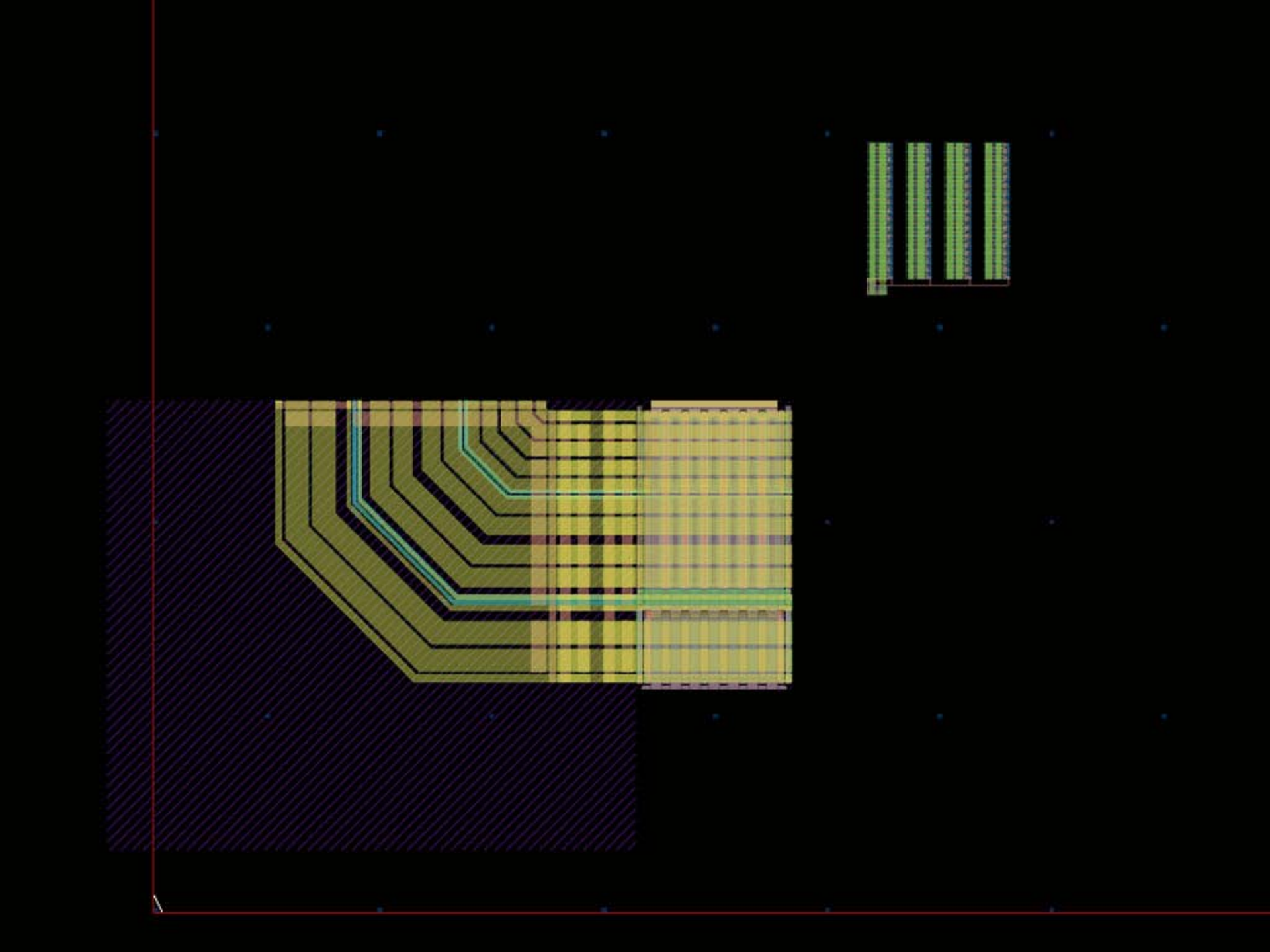












SV_tile5mmx5mm

SV_tile5mmx5mm_0

External Information Status

- Design Guidelines #6 Received
- SDK #6 with Patch 1 Received
- Top Metal Pattern Received
  - Communication between our two circuits
- Back Metal and Connection to Memory/Pads
  - Should be released soon
  - Tapeout 60 days after release (inc. holidays and weekends)
  - Quick Look Tapeout 45 days after release
  - Fab 20 weeks after tapeout

Testing

- Simulation
  - Verify test patterns
- Testbed
  - Programming
  - Run/Monitor Tests
- 3D CA
  - Operational Test
  - Functional/Application Tests

References

- MPW 100109 Design Guide, Revision 6, Tezzaron® Semiconductor, 4 November 2009, Available from MPW FTP Site
- FaStack Process Details, Revision 2, Tezzaron® Semiconductor, August 2009
  Available at
  http://tezzaron.com/technology/PDF/FaStack_Technology_2_0.pdf

Questions?