MCC MegaCell Compiler

- **Design, Build and Analyze Your Own Custom Memories.**
- **Process Independent Algorithmic Generators.**
- **Extract Verilog from Layout.**
- **Automatic Path Pruning reduces SPICE Deck by 1000X.**

The MegaCell Compiler (MCC) makes building all types of regular structures such as SRAMs, CAMs, DRAMs, Register Files, FIFOs, ROMs, PLAs, and even pad rings, fast and easy. The MegaCell Compiler is so fast that any size repetitive structure can be built in the comparable time it takes to load the data from the disk. Mere seconds for even multi-Mbit SRAMs.

Design and Build Custom Memories

MCC is a Designer's helper. It enables custom memory designers to quickly and easily construct and verify complete megacells from correct leaf cell layouts. MCC significantly reduces the effort required for full custom memory design.

More than just a simple tiler, MCC has a fully-hierarchical, relative-position tiling engine driven by a simple syntax. And if you don't want to create the syntax, simply arrange the instances in the desired configuration and MCC will tell you what syntax creates that configuration. Because the tiler is relative and uses the abutment boundaries of the cells themselves, process shrinks and even technology retargeting are effortless once the leaf cells have been migrated.

MCC also provides a new scheme for programming rows, mux's, etc., called via programming. Instead of relying on absolute coordinates; MCC automatically traces wire paths, finds overlaps, and automatically adds the appropriate vias.
To complete the megacell, MCC propagates ports from leaf cells to the top level and renames them

under programmatic control. Simply tell MCC to propagate the output ports on all of the sense amps, for example, and you get all of the ports from DOUT[0] to DOUT[31]. Because MCC handles tiling, via programming and port propagation, megacells are easily parameterizable. MCC's
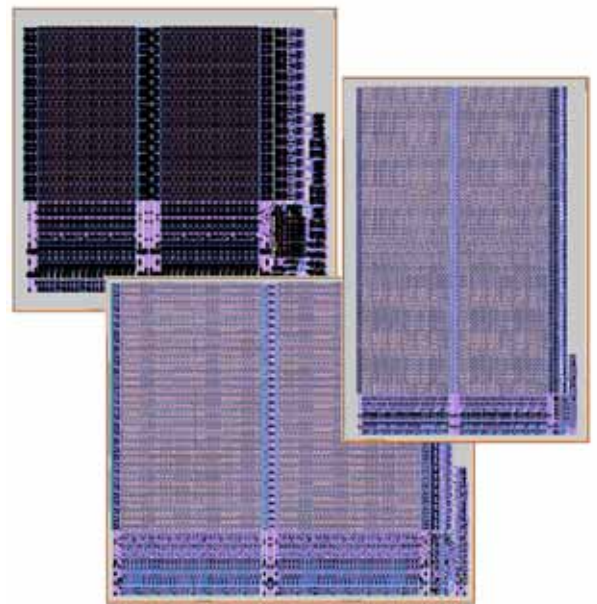

Figure 1-a.
Build a Family of SRAMs in a matter of minutes.

programming interface is so concise that a complete SRAM implementation takes less than 100 lines of code.

MCC allows the designer to parameterize the memory, i.e. build different sizes and configurations of the same basic memory structure simply by changing key parameters such as the number of rows or columns. This vastly speeds construction and verification, especially in large memory designs. By doing all construction and

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verification first on a very small structure, the iteration time is minimized. Only when the small structure passes do you go to the full size, which typically passes on the first try. Hence, parameterization helps irrespective of the number of final sizes/configurations desired.

Analyze and Verify Custom Memories

A big challenge in megacell design is verification, due to size and analog circuit techniques needed for high speed and low power. Physical, functional, performance, and noise analysis verification are all essential parts of all megacells. MCC extracts both complete SPICE and Verilog netlists of the finished megacells. In addition, MCC automatically extracts critical paths for performance evaluation.

In fact, MCC can create a compacted netlist of your megacell through any cell(s) that you select. This netlist is generated by tracing the cone of logic backwards to the input ports and forwards to the output ports from the selected cell(s), and prunes off unnecessary gates, resulting in a 1000x decrease in SPICE deck size. Thus if you select the memory cell that is furthest away from the decoders, you will get the longest path for the memory.

If you want to use third-party parasitic extraction tools, MCC will also output the layout of the cone of logic to a GDSII file.

MCC uses the Power of MAX

MCC runs from MAX, MMI's full custom layout editor, giving you all the power to view, edit and modify your megacells before and after creation. While MAX is ideal for creating the leaf cells, cells can also be imported through GDSII from other
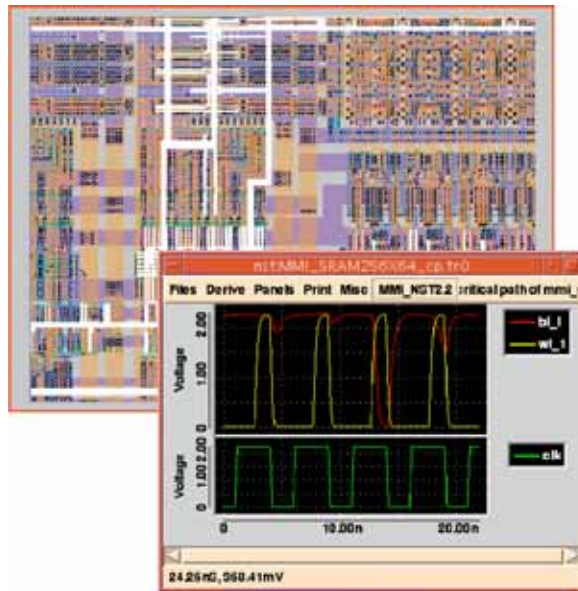

Figure 2-a.
View and analyze "critical" path for a megacell

layout editors. MCC and MAX provide full API support through the industry standard Tcl/Tk programming language.

MCC Features:

- Create user-configurable SRAMs, ROMs, CAMs, PLAs, DRAMs, FIFOs, Pad Rings, etc.
- Fully-hierarchical relative tiling engine.
- Via programming by tracing wire paths, NOT by specifying coordinates, saves thousands of lines of code and reduces errors.
- Very fast execution.
- Automatic Verilog netlisting directly from layouts means time-consuming LVS is no longer required.
- Easy to make fully parameterizable megacells.
- Completely technology independent.
- Automatic extraction of critical path netlists and layout.
- Ability to interface to industry-standard verification tools.
- Simple port propagation.
- Available on LINUX platforms.

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